AMENDMENT

In the Claims:

1. (Currently Amended) A DRAM IC comprising:

a first external connection to receive a first power supply voltage;

a second external connection to receive a second power supply voltage that is lower in voltage than the first power supply voltage;

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage; and

a second logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both ~~received~~ receive data to store within and output data retrieved from the selected memory cells, wherein the second logic is powered by the second power supply voltage;

wherein the first logic includes refresh logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the DRAM IC is placed in a lower power state in which the second logic is deprived of power as a result of the second power supply voltage being removed.

2. (Original) The DRAM IC of claim 1, wherein the first logic is coupled to the plurality of bit lines, and both transmits data across the plurality bit lines to the plurality of memory cells and receives data from across the plurality of bit lines from the memory cells.

3. (Original) The DRAM IC of claim 1, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

4. (Cancelled)

5. (Original) A DRAM IC comprising:

a first external connection to receive a first power supply voltage;

a second external connection to receive a second power supply voltage that is lower in voltage than the first power supply voltage;

a third external connection to receive a third power supply voltage that is lower in voltage than the first power supply voltage;

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage;

a second logic coupled to the first logic to control at least a portion of the first logic, wherein the second logic is powered by the second power supply voltage; and

a third logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both receive data to store within and output data retrieved from the selected memory cells, wherein the third logic is powered by the third power supply voltage.

6. (Original) The DRAM IC of claim 5, wherein the first logic is coupled to the plurality of bit lines, and both transmits data across the plurality bit lines to the plurality of memory cells and receives data from across the plurality of bit lines from the memory cells.

7. (Original) The DRAM IC of claim 5, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

8. (Previously Presented) The DRAM IC of claim 7, wherein the second logic is comprised of refresh logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the DRAM IC is placed in a lower power state in which the third logic is deprived of power as a result of the third power supply voltage being removed.

9. (Previously Presented) A memory device comprising:

a circuitboard;

a plurality of electrical contacts carried by the circuitboard to couple the circuitboard to a memory bus and to at least a first power supply voltage and a second power supply voltage; and

at least one DRAM IC comprising:

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage; and

a second logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both receive data to store within and output data retrieved from the selected memory cells, wherein the second logic is powered by the second power supply voltage;

wherein the first logic includes refresh logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the second logic is deprived of power as a result of the second power supply voltage being removed.

10. (Currently Amended) The memory device of claim 9, wherein the external interface of the at least one DRAM IC is directly coupled to at least a subset of the electrical contacts carried by the circuitboard to further couple the external interface of the at least one DRAM IC to the memory bus.

11. (Original) The memory device of claim 9, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

12. (Cancelled)

13. (Original) The memory device of claim 11, further comprising at least one interposed IC coupled to at least a subset of the electrical contacts carried by the

circuitboard and to the external interface of the at least one DRAM IC to at least buffer at least a subset of the signals communicated between the at least one DRAM IC and the memory bus, wherein the at least one interposed IC is powered by the second power supply voltage, and the at least DRAM IC carries out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the at least one interposed IC is deprived of power as a result of the second power supply voltage being removed.

14. (Original) A memory device comprising:

a circuitboard;

a plurality of electrical contacts carried by the circuitboard to couple the circuitboard to a memory bus and to at least a first power supply voltage, a second power supply voltage, and a third power supply voltage; and

at least one DRAM IC comprising:

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage;

a second logic coupled to the first logic to control at least a portion of the first logic, wherein the second logic is powered by the second power supply voltage; and

a third logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality

of memory cells for access, and to both receive data to store within and output data retrieved from the selected memory cells, wherein the third logic is powered by the third power supply voltage.

15. (Currently Amended) The memory device of claim 14, wherein the external interface of the at least one DRAM IC is directly coupled to at least a subset of the electrical contacts carried by the circuitboard to further couple the external interface of the at least one DRAM IC to the memory bus.

16. (Original) The memory device of claim 14, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

17. (Previously Presented) The memory device of claim 16, wherein the second logic is comprised of refresh logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the third logic is deprived of power as a result of the third power supply voltage being removed.

18. (Currently Amended) The memory device of claim 17, further comprising at least one interposed IC coupled to at least a subset of the electrical contacts carried by the circuitboard and to the external interface of the at least one DRAM IC to at least buffer at least a subset of the signals communicated between the at least one DRAM IC and the memory bus, wherein the at least one interposed IC is powered by the third power supply voltage, and the at least one DRAM IC carries out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower

power state in which the at least one interposed IC is deprived of power as a result of the third power supply voltage being removed.

19. (Currently Amended) An apparatus comprising:

a processor;

a core logic providing a memory controller coupled to the processor to provide a memory bus;

a first power source providing a first power supply voltage;

a second power source providing a second power supply voltage;

a power control circuit coupled to the core logic to selectively enable provision of the second power supply voltage; and

at least one DRAM IC comprising:

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage; and

a second logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both ~~received~~ receive data to store within and output data retrieved from the selected memory cells, wherein the second logic is powered by the second power supply voltage;

wherein the first logic includes refresh logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the

plurality of memory cells while the memory device is placed in a lower power state in which the second logic is deprived of power as a result of the second power supply voltage being removed by the power control circuit.

20. (Original) The apparatus of claim 19, wherein the external interface of the at least one DRAM IC is directly coupled to the memory bus.

21. (Original) The apparatus of claim 19, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

22. (Cancelled)

23. (Currently Amended) The apparatus of claim 21, further comprising at least one interposed IC coupled to at least a subset of the memory bus and to the external interface of the at least one DRAM IC to at least buffer at least a subset of the signals communicated between the at least one DRAM IC and the memory bus, wherein the at least one interposed IC is powered by the second power supply voltage, and the at least one DRAM IC carries out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the at least one interposed IC is deprived of power as a result of the second power supply voltage being removed by the power control circuit.

24. (Original) An apparatus comprising:

a processor;

a core logic providing a memory controller coupled to the processor to provide a memory bus;

a first power source providing a first power supply voltage;

a second power source providing a second power supply voltage;

a third power source providing a third power supply voltage;

a power control circuit coupled to the core logic to selectively enable provision of the third power supply voltage; and

at least one DRAM IC comprising:

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage;

a second logic coupled to the first logic to control at least a portion of the first logic, wherein the second logic is powered by the second power supply voltage; and

a third logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both receive data to store within and output data retrieved from the selected memory cells, wherein the third logic is powered by the third power supply voltage.

25. (Original) The apparatus of claim 24, wherein the external interface of the at least one DRAM IC is directly coupled to the memory bus.

26. (Original) The apparatus of claim 24, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

27. (Original) The apparatus of claim 26, wherein the second logic is comprised of refresh logic control the at least a portion of the first logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the third logic is deprived of power as a result of the third power supply voltage being removed by the power control circuit.

28. (Currently Amended) The apparatus of claim 27, further comprising at least one interposed IC coupled to at least a subset of the electrical contacts carried by the circuitboard and to the external interface of the at least one DRAM IC to at least buffer at least a subset of the signals communicated between the at least one DRAM IC and the memory bus, wherein the at least one interposed IC is powered by the third power supply voltage, and the at least one DRAM IC carries out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the at least one interposed IC is deprived of power as a result of the third power supply voltage being removed by the power control circuit.

29. (Original) A method comprising:

signaling a memory device to enter into a lower power state, wherein the memory device is comprised of a plurality of memory cells organized into at least one two-dimensional array of rows and columns, a first logic to at least transmit signals to the memory cells and second logic to provide an external interface, wherein the memory cells

and the first logic are powered by the first power supply voltage, and wherein the second logic is powered by the second power supply voltage;

depriving the second logic of power by removing the second power supply voltage;

carrying out at least one refresh operation wherein the first logic signals a row of the plurality of the memory cells through a word line to which the row of the plurality of memory cells and the first logic are coupled;

restoring the second power supply voltage to the second logic by providing the second power supply voltage; and

signaling the memory device to exit the lower power state.

30. (Original) The method of claim 29, further comprising:

depriving an interposed IC of power by removing the second power supply voltage at substantially the same time that power is removed from the second logic, wherein the interposed IC is coupled to the external memory interface of the memory device and is powered by the second power supply voltage; and

restoring power to the interposed IC by providing the second power supply voltage.

31. (Original) A machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to:

signal a memory device to enter into a lower power state, wherein the memory device is comprised of a plurality of memory cells organized into at least one two-dimensional array of rows and columns, a first logic to at least transmit signals to the memory cells and second logic to provide an external interface, wherein the memory cells and the first logic are powered by the first power supply voltage, and wherein the second logic is powered by the second power supply voltage;

deprive the second logic of power by removing the second power supply voltage;

signal the first logic to carry out at least one refresh operation wherein the first logic signals a row of the plurality of the memory cells through a word line to which the row of the plurality of memory cells and the first logic are coupled;

restore the second power supply voltage to the second logic by providing the second power supply voltage; and

signaling the memory device to exit the lower power state.

32. (Original) The machine-accessible medium of claim 31, further causing the processor to:

deprive an interposed IC of power by removing the second power supply voltage at substantially the same time that power is removed from the second logic, wherein the interposed IC is coupled to the external memory interface of the memory device and is powered by the second power supply voltage; and

restore power to the interposed IC by providing the second power supply voltage.